sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter;

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and a level represented by the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,

wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter,

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and the first threshold level, the second read reference parameter is allocated to represent a level between the first threshold level and the second threshold level, and the third read reference parameter is allocated to represent a level between the second threshold level and the third threshold level, and

wherein the level represented by the second read reference parameter is allocated substantially at a midpoint between the first threshold level and the second threshold level, and the level represented by the first read reference parameter is allocated toward the first threshold level from a midpoint between the threshold level indicating the erase state and the first threshold level.

108.(New) A non-volatile semiconductor memory device according to claim 107,

wherein an operation of shifting the one non-volatile memory cell threshold voltage to the threshold level indicating the selected programming state includes a program operation in which electrons are injected into the floating gate of the one non-volatile memory cell by applying at least one programming pulse to a bit line coupled to a drain of the one non-volatile memory cell.

109.(New) A non-volatile semiconductor memory device according to claim 107,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

110.(New) A non-volatile semiconductor memory device according to claim 109,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

111.(New) A non-volatile semiconductor memory device according to claim 108,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

112.(New) A non-volatile semiconductor memory device according to claim 111, wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

113.(New) A non-volatile semiconductor memory device comprising:

a plurality of non-volatile memory cells each of which has a floating gate and a threshold voltage representing data of at least two bits, wherein electrons are capable of being injected into the floating gate, and wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and

sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read

reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter;

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and a level represented by the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,

wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the

information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter representing the threshold voltage of the one non-volatile memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter,

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and the first threshold level, the second read reference parameter is allocated to represent a level between the first threshold level and the second threshold level, and the third read reference parameter is allocated to represent a level between the second threshold level and the third threshold level, and

wherein the level represented by the second read reference parameter is allocated substantially at a midpoint between the first threshold level and the second threshold level, and the level represented by the third read reference parameter is allocated toward the second threshold level from a midpoint between the second threshold level and the third threshold level.

114.(New) A non-volatile semiconductor memory device according to claim 113, wherein an operation of shifting the one non-volatile memory cell threshold voltage to the threshold level indicating the selected programming state includes a program operation in which electrons are injected into the floating gate of the one non-volatile memory cell by applying at least one programming pulse supplied to a bit line coupled to a drain of the one non-volatile memory cell.

115. A non-volatile semiconductor memory device according to claim 113,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

116. A non-volatile semiconductor memory device according to claim 115,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

117. A non-volatile semiconductor memory device according to claim 114,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

118. A non-volatile semiconductor memory device according to claim 117,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

119. A non-volatile semiconductor memory device comprising:

a plurality of non-volatile memory cells each of which has a floating gate and a threshold voltage representing data of at least two bits, wherein electrons are capable of being injected into the floating gate, and wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and

sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read

reference parameter, a third programming reference parameter and a third read reference parameter;

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and a level represented by the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,

wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the

information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter representing the threshold voltage of the one non-volatile memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter,

wherein the first read reference parameter is allocated to represent a level between the threshold level indicating the erase state and the first threshold level, the second read reference parameter is allocated to represent a level between the first threshold level and the second threshold level, and the third read reference parameter is allocated to represent a level between the second threshold level and the third threshold level, and

wherein the level represented by the second read reference parameter is allocated substantially at a midpoint between the first threshold level and the second threshold level, and the level represented by the first read reference parameter is allocated toward the first threshold level from a midpoint between the threshold level indicating the erase state and the first threshold level, and the level represented by the third read reference parameter is allocated toward the second threshold level from a midpoint between the second threshold level and the third threshold level.

120. A non-volatile semiconductor memory device according to claim 119,

wherein an operation of shifting the one non-volatile memory cell threshold voltage to the threshold level indicated the selected programming state includes a program operation in which electrons are injected into the floating gate of the one non-volatile memory cell by applying at least one programming pulse supplied to a bit line coupled to a drain of the one non-volatile memory cell.

121.(New) A non-volatile semiconductor memory device according to claim 119,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

122.(New) A non-volatile semiconductor memory device according to claim 121,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

123.(New) A non-volatile semiconductor memory device according to claim 120,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

124.(New) A non-volatile semiconductor memory device according to claim 123,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.--